



INTEGRATED TECHNICAL EDUCATION CLUSTER  
AT ALAMEERIA

**E-626-A**

**Real-Time Embedded Systems (RTES)**

Lecture #8

Data acquisition and manipulation

ADC & DAC

**Instructor:**

**Dr. Ahmad El-Banna**



# Agenda



Digital, Analog signals & Acquisition

ADC

DAC

# Analog and digital quantities

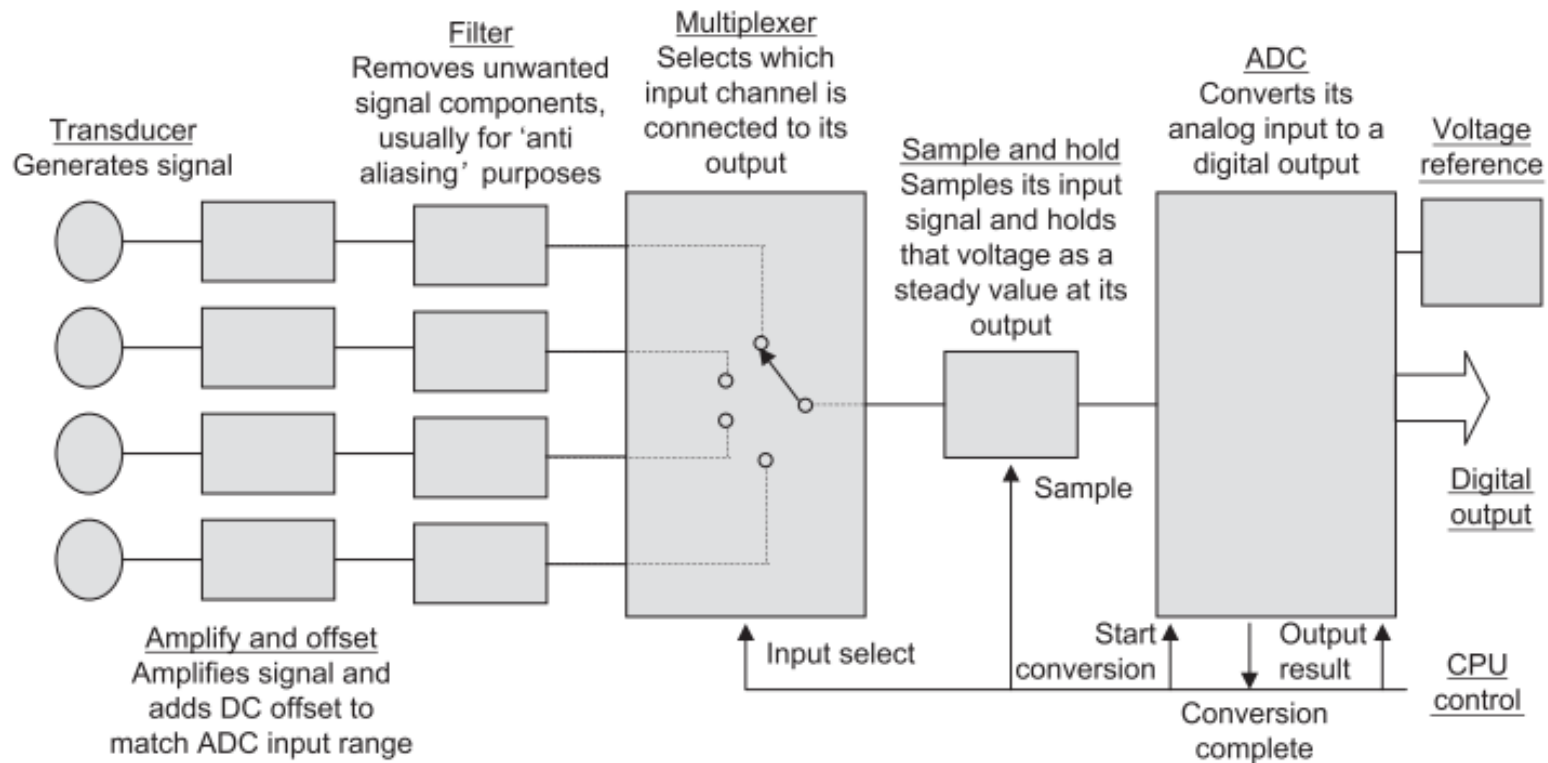
- Most **transducers** produce output signals that are an **analog** of the quantity they represent.
- For **example**: Temperature sensors & microphones.
- **Analog** signals are fine things, but they suffer from a number of big **disadvantages**.
- **Digital** signals, on the other hand, perform **better** on most counts and with today's technology are easier to work with.

# Some properties of analog and digital quantities

Property	Analog	Digital
Means of (electrical) representation	A continuously variable voltage, or current, represents the variable.	Variable is represented by a binary number.
Precision of representation	Can take an infinite range of values; absolute precision is theoretically possible, as long as the signal is kept completely uncorrupted.	Only a fixed number of digit combinations are available to represent measure; for example, an 8 bit number has only 256 different combinations. 'Continuously variable' quality of analog signal cannot be replicated.
Resistance to signal degradation	Almost inevitably suffers from drift, attenuation, distortion, interference. Cannot completely recover from these.	Digital representation is intrinsically tolerant of most forms of signal degradation. Error checking can also be introduced and with appropriate techniques complete recovery of a corrupted signal can be possible.
Processing	Analog signal processing using op amps and other circuits has reached sophisticated levels, but is ultimately limited in flexibility and always suffers from signal degradation.	Fantastically powerful computer based techniques available.
Storage	Genuine analog storage for any length of time is almost impossible.	All major semiconductor memory technologies are digital.

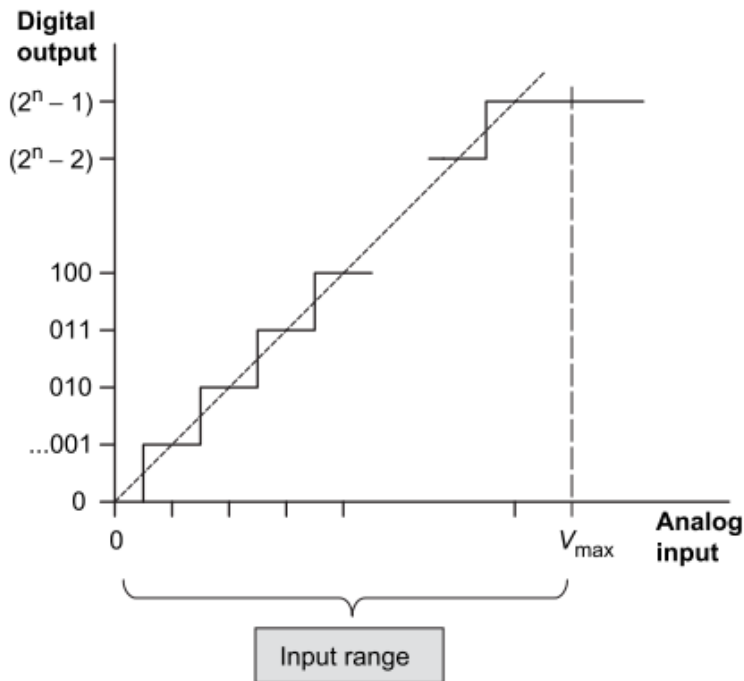
# The data acquisition system

- Elements of a (four-channel) data acquisition system

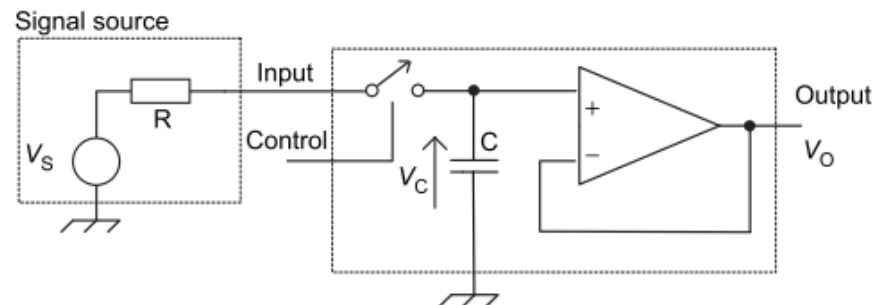


# ADC ch/s

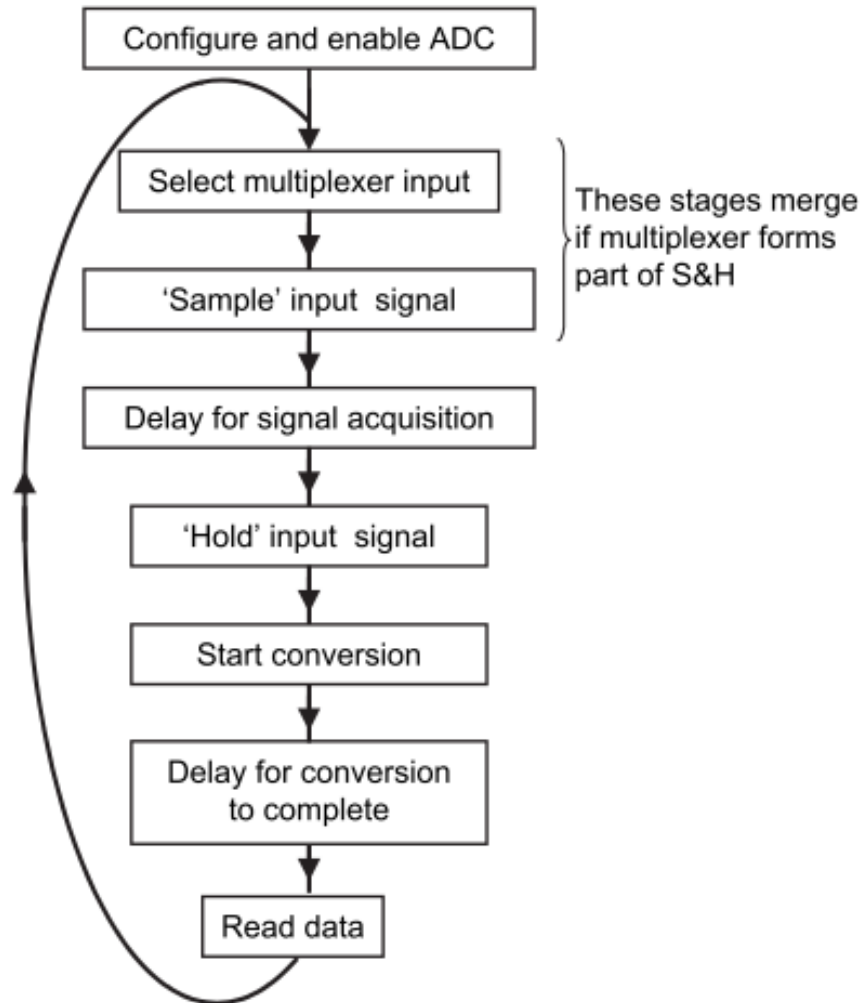
- The ideal analog-to-digital converter input/output characteristic



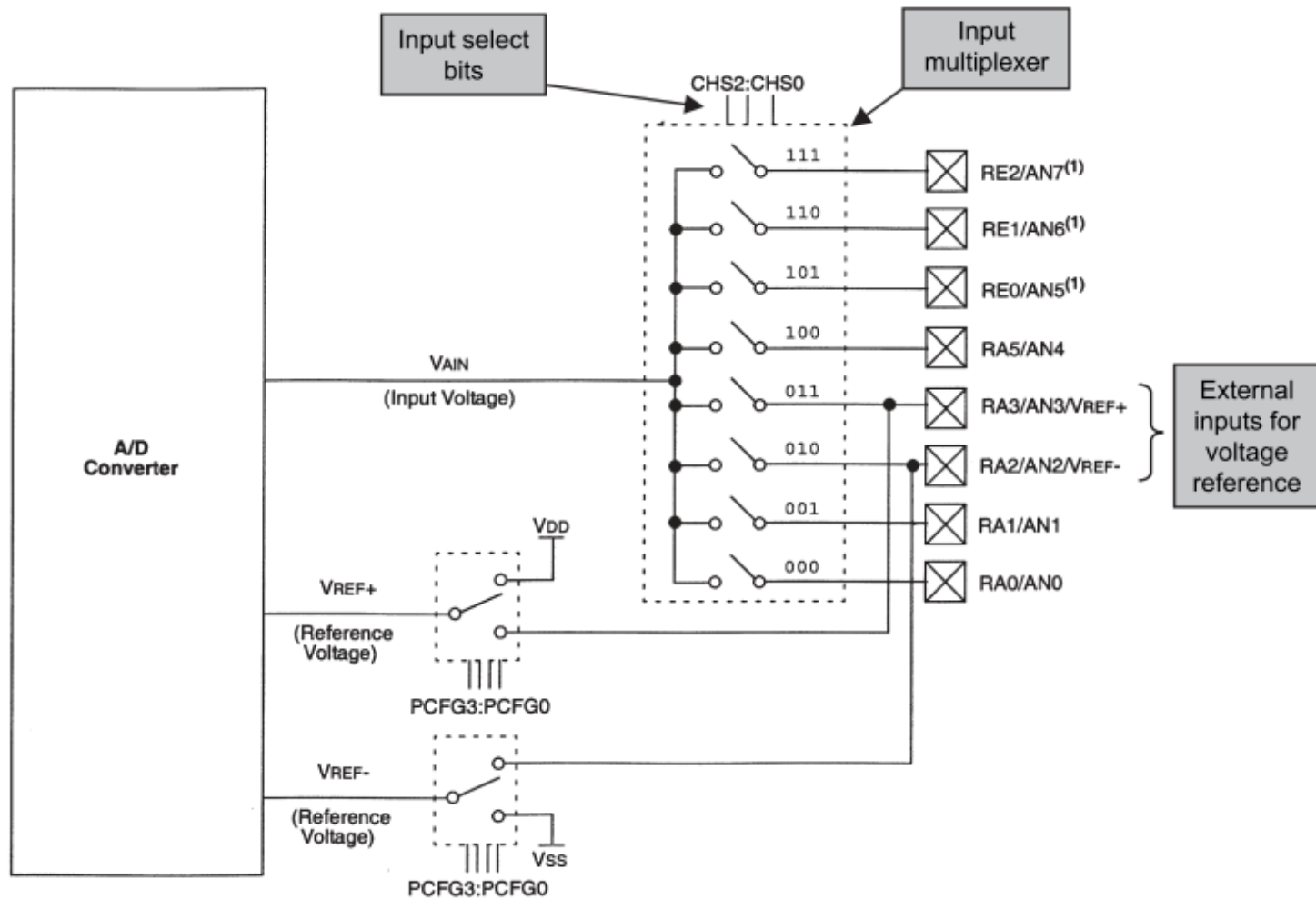
- Sample & Hold Circuit



# Typical timing requirement of one analog-to-digital conversion



# The PIC 16F87XA ADC module



**Note 1:** Not available on 28-pin devices.



# Controlling the ADC

- The ADC is controlled by two SFRs, ADCON0 and ADCON1).
- The result of the conversion is placed in two further SFRs, ADRESH and ADRESL.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit 7						bit 0	

bit 7-6 **ADCS1:ADCS0**: A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0**: Analog Channel Select bits

000 = Channel 0 (AN0)  
 001 = Channel 1 (AN1)  
 010 = Channel 2 (AN2)  
 011 = Channel 3 (AN3)  
 100 = Channel 4 (AN4)  
 101 = Channel 5 (AN5)  
 110 = Channel 6 (AN6)  
 111 = Channel 7 (AN7)

**Note:** The PIC16F873A/876A devices only implement A/D channels 0 through 4; the unimplemented selections are reserved. Do not select any unimplemented channels with these devices.

bit 2 **GO/DONE**: A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)  
 0 = A/D conversion not in progress

bit 1 **Unimplemented**: Read as '0'

bit 0 **ADON**: A/D On bit

1 = A/D converter module is powered up  
 0 = A/D converter module is shut-off and consumes no operating current

The ADCON0 register  
(address 1F H )



# The ADCON1 register (address 9F H )

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7				bit 0			

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.  
0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in shaded area and in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented:** Read as '0'

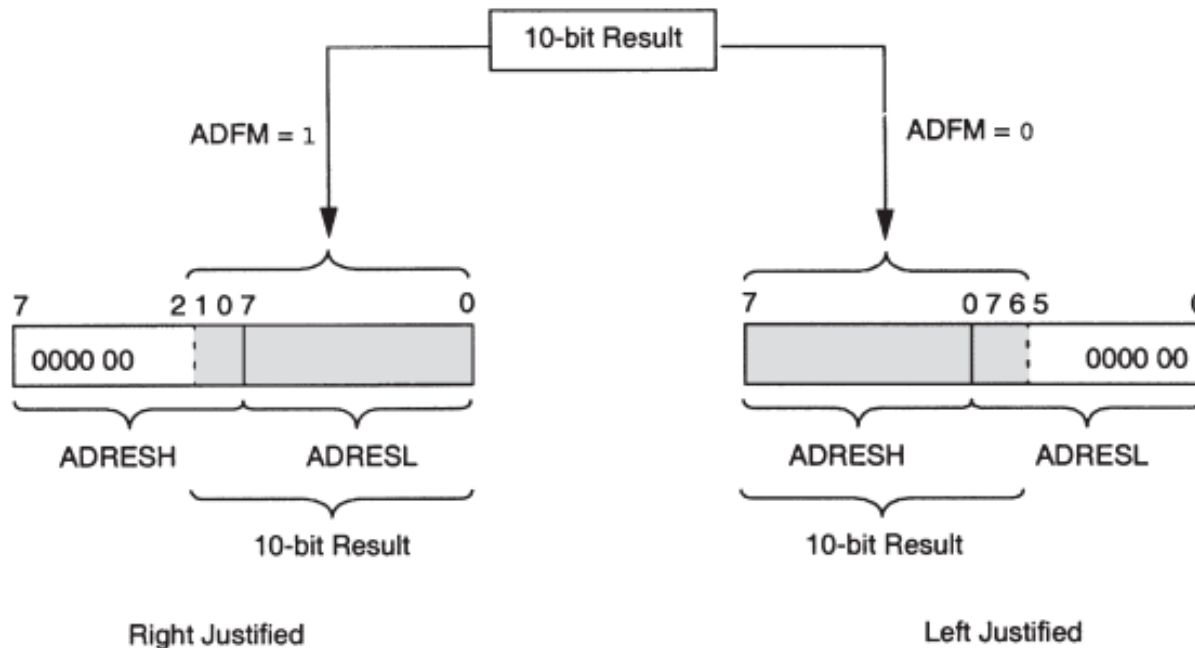
bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2/1
011x	D	D	D	D	D	D	D	D	—	—	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1/2

A = Analog input D = Digital I/O

C/R = # of analog input channels/# of A/D voltage references

# Formatting the analog-to-digital converter conversion result



- **Calculating acquisition time**

$$t_{ac} = \text{Amplifier setting time} + \text{Hold capacitor charging time} + \text{Temperature coefficient}$$

$$\text{Temperature coefficient} = (\text{Temperature} - 25^{\circ}\text{C})(0.05 \mu\text{s}/^{\circ}\text{C})$$

# DAC

- The reverse function of ADC.
- Needs external interface circuit.
- Convert digital values into continuous analogue signal
  - Decoding digital value to an analogue value at discrete moments in time based on value within register

$$E_0 = E_{ref} \left\{ 0.5B_1 + 0.25B_2 + \dots + (2^n)^{-1} B_n \right\}$$

Where  $E_0$  is output voltage;  $E_{ref}$  is reference voltage;  $B_n$  is status of successive bits in the binary register

# Examples of DAC Circuits

- Scaling Adder as a four-digit DAC

$$I_0 = +V/8R$$

$$I_1 = +V/4R$$

$$I_2 = +V/2R$$

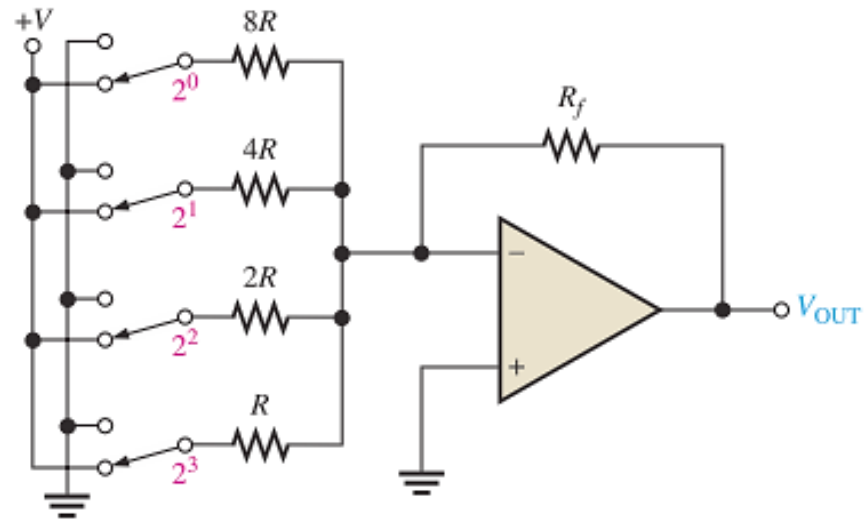
$$I_3 = +V/R$$

$$V_{out(D0)} = -R_f I_0$$

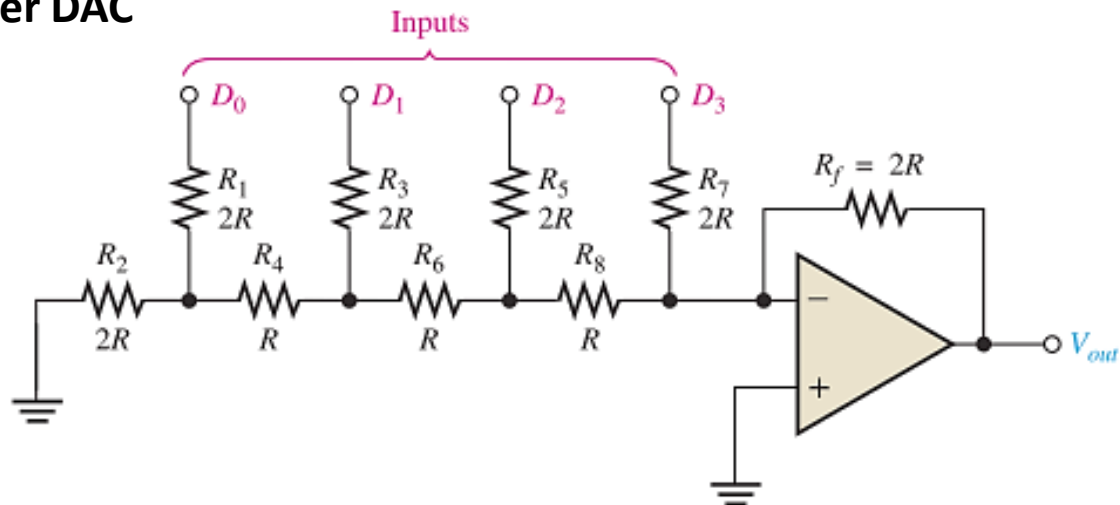
$$V_{out(D1)} = -R_f I_1$$

$$V_{out(D2)} = -R_f I_2$$

$$V_{out(D3)} = -R_f I_3$$



- An R/2R ladder DAC



# Sample Project

- Design and implement a digital voltmeter.

- For more details, refer to:
  - Chapter 11, T. Wilmishurst, **Designing Embedded Systems with PIC Microcontrollers**, 2010.
- The lecture is available online at:
  - <http://bu.edu.eg/staff/ahmad.elbanna-courses/12134>
- For inquires, send to:
  - [ahmad.elbanna@feng.bu.edu.eg](mailto:ahmad.elbanna@feng.bu.edu.eg)